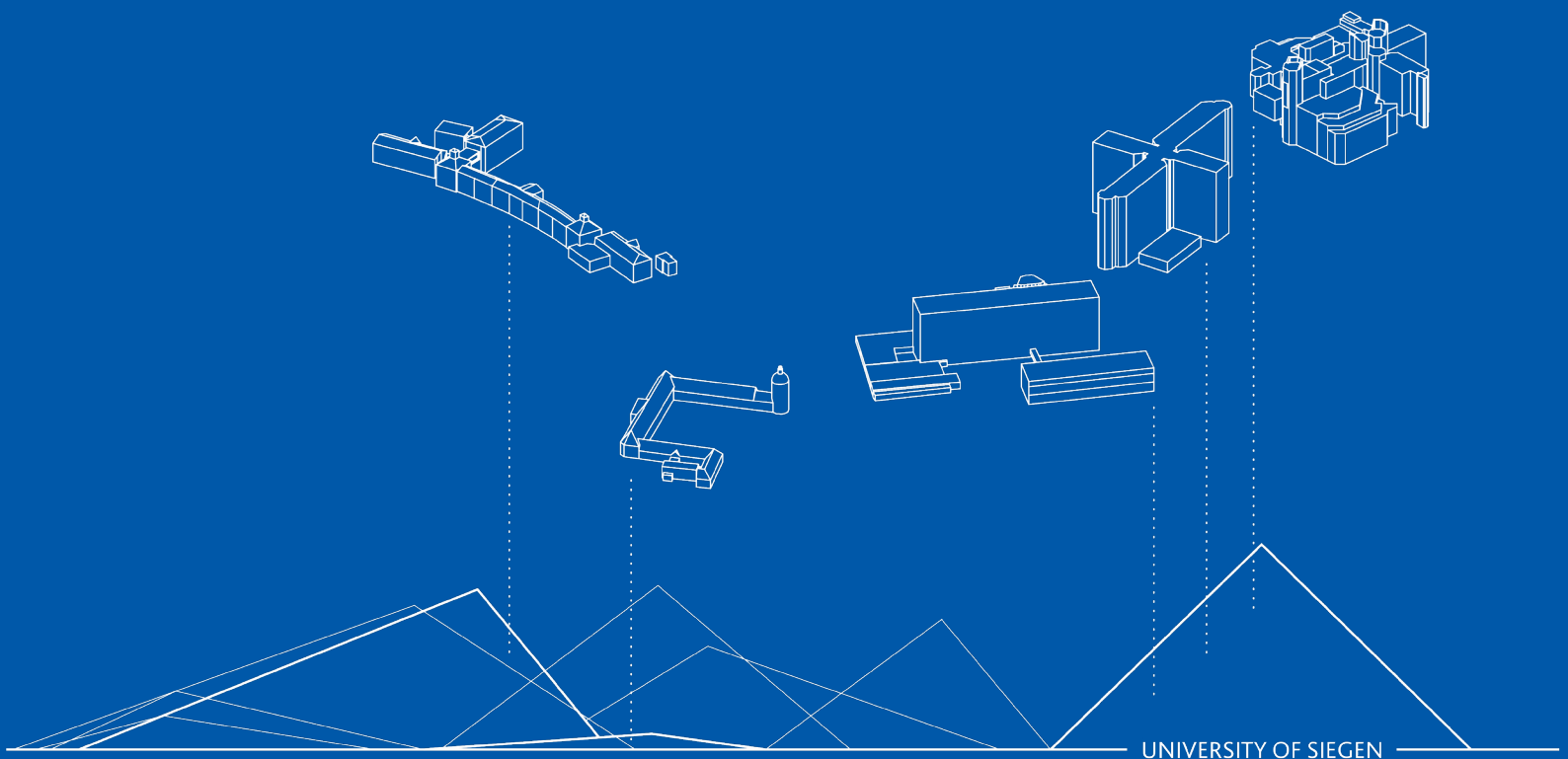

SPI 2021

25th IEEE Workshop On Signal And Power Integrity

May 10-12, 2021 - Virtual Online Conference

www.spi-conference.org ✉ spi@uni-siegen.de

Organized by

University of Siegen, Siegen, Germany

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25th IEEE Workshop On Signal And Power Integrity

Conference Guide

Time*	Monday, 10.05.	Time	Tuesday, 11.05.	Time	Wednesday, 12.05.
13:00	Opening Session	13:00	Keynote	13:00	Tutorial - Part 2
13:15	Tutorial - Part 1	13:40	Industry presentation DASSAULT SYSTEMES	14:00	The IEEE Packaging Benchmarks Initiative
14:15	Industry presentation KEYSIGHT TECHNOLOGIES	14:00 (4.1)	High Speed Design and Signal Integrity Analysis 1	14:10 (7.1)	Stochastic Analysis and Uncertainty Quantification 1
14:35 Session (1.1)	Design Methodology for Signal and Power Integrity Analysis 1	15:00	Short Break	14:50	Short Break
15:35	Short Break	15:05	Industry presentation KEYSIGHT TECHNOLOGIES	14:55 (7.2)	Stochastic Analysis and Uncertainty Quantification 2
15:40 (1.2)	Design Methodology for Signal and Power Integrity Analysis 2	15:25 (4.2)	High Speed Design and Signal Integrity Analysis 2	15:35	Closing Session
16:20	Industry presentation ROHDE&SCHWARZ	16:05 (4.3)	High Speed Design and Signal Integrity Analysis 3		
16:40 (2)	Measurement and Characterization	16:45	Short Break	16:00	IBIS Summit
17:20	Short Break	16:50 (5)	Macro-Modeling		
17:25 (3)	Advanced Interconnect Technologies	17:50 (6)	Design Support by Machine Learning and Artificial Intelligence		

*all times are CEST

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25th IEEE Workshop On Signal And Power Integrity

Tutorials

Tutorial - Demystifying Machine Learning for Signal and Power Integrity Applications

Part 1: Monday, 13:15 - Riccardo Trinchero - Politecnico di Torino, Torino (ITA)

Part 2: Wednesday, 13:00 - Madhavan Swaminathan - Georgia Institute of Technology, Atlanta (USA)

Abstract

During last years' Machine Learning (ML) approaches have been successfully applied to several realistic scenarios belonging to different research fields, including Signal Integrity (SI) & Power Integrity (PI) applications. The aim of this tutorial is twofold. On one hand, it will cover some of the basic principles of ML regression techniques. Key concepts such as: the learning paradigm, overfitting/underfitting, regularization, the "kernel trick" will be presented in an intuitive way with the help of illustrative examples. On the other hand, the second part of the tutorial will investigate the effectiveness and the strength of ML techniques for the optimization and the uncertainty quantification in real and advanced SI/PI applications. Several case studies will be presented to compare the performances of ML technique with respect to well-established state-of-the-art approaches.

Speakers

Riccardo Trinchero received the M.Sc. and the Ph.D. degrees in Electronics and Communication Engineering from Politecnico di Torino, Torino, Italy, in 2011 and 2015, respectively. He is currently an Assistant Professor within the EMC Group with the Department of Electronics and Telecommunications at the Politecnico di Torino. His research interests include the analysis of switching DC-DC converters, machine learning and statistical simulation of circuits and systems.

Madhavan Swaminathan is the John Pippin Chair in Microsystems Packaging & Electromagnetics in the School of Electrical and Computer Engineering (ECE), Professor in ECE with a joint appointment in the School of Materials Science and Engineering (MSE), and Director of the 3D Systems Packaging Research Center (PRC), Georgia Tech (GT) (http://www.prc.gatech.edu). He also serves as the Site Director for the NSF Center for Advanced Electronics through Machine Learning (CAEML) and Theme Leader for Heterogeneous Integration, at the SRC JUMP ASCENT Center. He formerly held the positions of Founding Director, Center for Co-Design of Chip, Package, System (C3PS), Joseph M. Pettit Professor in Electronics in ECE, and Deputy Director of the Packaging Research Center (NSF ERC), GT. Prior to joining GT, he was with IBM working on packaging for supercomputers.

He is the author of 500+ refereed technical publications and holds 31 patents. He is the primary author and co-editor of 3 books and 5 book chapters, founder and co-founder of two start-up companies, and founder of the IEEE Conference on Electrical Design of Advanced Packaging and Systems (EDAPS), a premier conference sponsored by the IEEE Electronics Packaging Society (EPS). He is an IEEE Fellow and has served as the Distinguished Lecturer for the IEEE Electromagnetic Compatibility (EMC) society.

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25th IEEE Workshop On Signal And Power Integrity

Keynote

Keynote - Future Trends on Interconnects for High End Servers

Tuesday, 13:00 - Hubert Harrer (IBM)

Abstract

The talk will give an overview on industry trends with respect to packaging technologies and interconnects. It will start with an overview on the development of chip technology and the resulting challenges on chip-to-chip interconnects. The trend of high speed IOs in high end servers will be shown and design impact examples will be given. Different options for system integration will be explained. The co-optimization of chip, package and overall system aspects will get increased importance in the future. This optimization does lead to different solutions with respect to single-chip modules, multi-chip modules or other hybrid integration technologies depending on architecture and other boundary conditions. The tremendous increase on signal speed is changing the traditional board and card design. Moving to PAM4 the small vertical eye openings will not tolerate any larger crosstalk sources in the design like coupling from through vias or impedance mismatches caused by connectors. This is driving changes and new requirements for signal and power integrity including their design tools.

Speaker

Hubert Harrer is a Senior Technical Staff Member (STSM) working in the IBM Systems Group. He received his Dipl.-Ing. degree in 1989 and his Ph.D. degree in 1992 from the Technical University of Munich. In 1993 he received a DFG (Deutsche Forschungsgemeinschaft) research grant to work at the University of California at Berkeley in the paradigm of Cellular Neural Networks.

Since 1994 he has worked for IBM in the Boeblingen Packaging Department. In 1999 he was on international assignment at IBM Poughkeepsie, New York. He is the technical lead for IBM z electronic packaging integration. This includes the systems z900, z990, z9, z10, z196, EC12, z13, z14 and z15 mainframe computers. His technical interests focus on system architecture and design, packaging technology, high frequency designs and electrical analysis for first and second level packaging. He has published multiple papers and patents on packaging.

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SPI 2021

25th IEEE Workshop On Signal And Power Integrity

Conference Program (1/5)

Monday, May 10th, 2021 (1/2)

13:00 **Opening Session**

13:15 **Tutorial - Part 1: Demystifying Machine Learning for Signal and Power Integrity Applications**
Riccardo Trinchero - Politecnico di Torino, Torino (ITA)

14:15 **Industry Presentation**
Keysight Technologies

Session 1.1 **Design Methodology for Signal and Power Integrity Analysis 1**
Chair: Uwe Arz, Physikalisch-Technische Bundesanstalt, Braunschweig (GER)

14:35 **Bayesian Optimization of Hyperparameters in Kernel-Based Delay Rational Models**
F. Treviso, R. Trinchero, F. G. Canavero

14:50 **Fast and Stable Transient Simulation of Nonlinear Circuits using the Numerical Inversion of the Laplace Transform**
B. Bandali, E. Gad, M. Nakhla

15:05 **An Automated Framework for Variability Analysis using Simulated Annealing**
A. Chordia, S. Hemaram, J. N. Tripathi

This session is brought to you by KEYSIGHT TECHNOLOGIES

15:35 **Short Break**

1.2 **Design Methodology for Signal and Power Integrity Analysis 2**
Chair: Stefano Grivet-Talocia, Politecnico di Torino, Torino (ITA)

15:40 **A Compact and Broadband On-Chip Delay Line Design Based on the Bridged T-Coil**
S. R. Mahendraand, A. Weisshaar

15:55 **PCB Analysis Method by S-Parameters for Power Inverters with GaN Devices in Parallel**
R. Franchino, R. Mitova

This session is brought to you by KEYSIGHT TECHNOLOGIES

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25th IEEE Workshop On Signal And Power Integrity

Conference Program (2/5)

Monday, May 10th, 2021 (2/2)

16:20 **Industry Presentation**
Rohde & Schwarz

ROHDE&SCHWARZ

Session 2 **Measurement and Characterization**
Chair: Flavio G. Canavero, Politecnico di Torino, Torino (ITA)

16:40 **Non-destructive PCB Substrate Height Extraction with Multi-Measurement Technique**
T. Wang Lee, F. de Paulis, M. Resso, M. Piket-May, E. Bogatin

16:55 **Impact of Chuck Boundary Conditions on Wideband On-Wafer Measurements**
G. N. Phung, U. Arz

This session is brought to you by ROHDE&SCHWARZ

17:20 **Short Break**

3 **Advanced Interconnect Technologies**
Chair: Christian Schuster, Hamburg University of Technology, Hamburg (GER)

17:25 **Electrothermal Modeling and Characterization of Graphene-Based Thin Strips**
A. Maffucci, L. Ferrigno, S. Sibilia, F. Bertocchi, S. Chiodini, F. Cristiano, G. Giovinco

17:40 **Investigation of an Integrated Directional Coupler Manufactured by a Field-Assisted Diffusion Process**
D. Uebach, T. Kühler and E. Griese

17:55 **De-mystifying the impact of Intra-pair Skew on high-speed SerDes Interconnect**
H. Dsilva, S. McMorrow, A. Gregory,S. Krooswyk, R. Mellitz, B. Lee

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SPI 2021

25th IEEE Workshop On Signal And Power Integrity

Conference Program (3/5)

Tuesday, May 11th, 2021 (1/2)

13:00 **Keynote - Future Trends On Interconnects For High End Servers**
Hubert Harrer (IBM)

13:40 **Industry Presentation**
3DS

Session 4.1 **High Speed Design and Signal Integrity Analysis 1**
Chair: Hartmut Grabinski, Leibniz University Hannover, Hannover (GER)

14:00 **The Sensitivity of ENRZ to skew – In Comparison to NRZ, PAM3, and PAM4**
S. S. Chen, Z. Xu

14:15 **High Density RRAM Arrays with Improved Thermal and Signal Integrity**
K. Lahbacha, H. Belgacem, W. Dghais, F.Zayer, A. Maffucci

14:30 **Error Propagation in Channel Operating Margin**
L. Bai

This session is brought to you by DASSAULT SYSTEMES

15:00 **Short Break**

15:05 **Industry Presentation**
Keysight Technologies

4.2 **High Speed Design and Signal Integrity Analysis 2**
Chair: Mihai Telescu, Université de Bretagne Occidentale, Brest (FRA)

15:25 **Intra-Pair Skew Metric, EIPS (Effective Intra-Pair Skew)**
S.-J. Moon, J., X. Zhang, C.-P. Kao, B. Lee, H. Dsilva, J.-R. Guo

15:40 **Analysis of Differential Crosstalk and Transmission for Via Arrays in Low Temperature Cofired Ceramics**
Ö. F. Yildiz, N. Pathé, M. Bochard, C. Yang, C. Schuster

This session is brought to you by KEYSIGHT TECHNOLOGIES

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25th IEEE Workshop On Signal And Power Integrity

Conference Program (4/5)

Tuesday, May 11th, 2021 (2/2)

Session 4.3 **High Speed Design and Signal Integrity Analysis 3**
Chair: Madhavan Swaminathan, Georgia Institute of Technology, Atlanta (USA)

16:05 **Generalized ccICN (component contribution Integrated Crosstalk Noise) for PAM-N**
S.-J. Moon, Z. Wu, M. Mazumder

16:20 **Distributed PDN Modeling Approach for Accurate Jitter Estimation in High-Speed NAND Flash Memory**
S. Mobin, P. Balachander, A. Sharma, J. Lee, V. Ramachandra, C. D. Nguyen

16:45 Short Break

5 **Macro-Modeling**
Chair: Antonio Maffucci, University of Cassino and Southern Lazio, Cassino (ITA)

16:50 **A Multivariate Adaptive Sampling Scheme for Passivity Characterization of Parameterized Macromodels**
M. De Stefano, S. Grivet-Talocia

17:05 **A Tunable Macro-Modeling Method for Signal Transition in mm-Wave Flip-Chip Technology**
P. Namaki, M.-R. Nezhad-Ahmadi, N. Masoumi, S. Safavi-Naeini

17:20 **Macro-modeling and the Parameter Fitting Method for Switching Noise of Buck Converter IC**
A. Huang, S. PK, S. Singh, B. Mutnury, J. Drewniak, C. Hwang

6 **Design Support by Machine Learning and Artificial Intelligence**
Chair: Thomas Kühler, University of Siegen, Siegen (GER)

17:50 **Comparative study of Machine Learning methods for variability analysis in High-speed link**
T. Nguyen, B. Shi, J. Schutt-Aine

18:05 **Machine Learning-Based Verilog-A Modeling for Power Distribution Network of On-Die Regulator**
M. Chang, S. Kao, S. Chu, B. Hsu, M. Ciou, K. Chung, R. Ho

18:20 **ANN Hyperparameter Optimization by Genetic Algorithms for Via Interconnect Classification**
A. Sánchez-Masís, A. Carmona-Cruz, M. Schierholz, X. Duan, K. Roy, C. Yang, R. Rimolo-Donadio, C. Schuster

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SPI 2021

25th IEEE Workshop On Signal And Power Integrity

Conference Program (5/5)

Wednesday, May 12th, 2021

13:00 Tutorial - Part 2: Demystifying Machine Learning for Signal and Power Integrity Applications
Madhavan Swaminathan - Georgia Institute of Technology, Atlanta (USA)

14:00 The IEEE Packaging Benchmarks Initiative: An Overview
Stefano Grivet-Talocia, Politecnico di Torino, Torino (ITA)

This talk will provide a brief update on the most recent activities of the IEEE Electronic Packaging Society Technical Committee on Electrical Design, Modeling and Simulation, with emphasis on the Packaging Benchmark initiative. This project maintains a public repository of packaging benchmarks (http://www.packaging-benchmarks.org) of various levels of complexity, hoping to provide users from academia, tool vendors and companies a set of peer-reviewed and validated modeling and simulation problems (including full layout) for research purposes.

Session 7.1 **Stochastic Analysis and Uncertainty Quantification 1**
Chair: José E. Schutt-Ainé, University of Illinois, Urbana-Champaign (USA)

14:10 **A Multi-Fidelity Polynomial Chaos Approach for Uncertainty Quantification of MWCNT Interconnect Networks in the Presence of Imperfect Contacts**
S. Guglani, KM Dimple, B. K. Kaushik, S. Roy, R. Sharma

14:25 **A Nonparametric Surrogate Model for Stochastic Crosstalk Analysis Including Confidence Bounds**
P. Manfredi, R. Trinchero

14:50 Short Break

7.2 **Stochastic Analysis and Uncertainty Quantification 2**
Chair: Michel S. Nakhla, Carleton University, Ottawa (CAN)

14:55 **Stochastic Analysis Method for Tree-Type PDNs on Mixed-Signal PCB**
M. Mehri

15:10 **Uncertainty Quantification of Memristor Crossbar Array for Vector Matrix Multiplication**
R. Kumar, A. Chordia, A. AR, A. James, J. N. Tripathi

15:35 Closing Session

16:00 IBIS Summit